551546

New Instrumentation, Patterns and Their Effects on TID Testing of Antifuse - Based FPGAs

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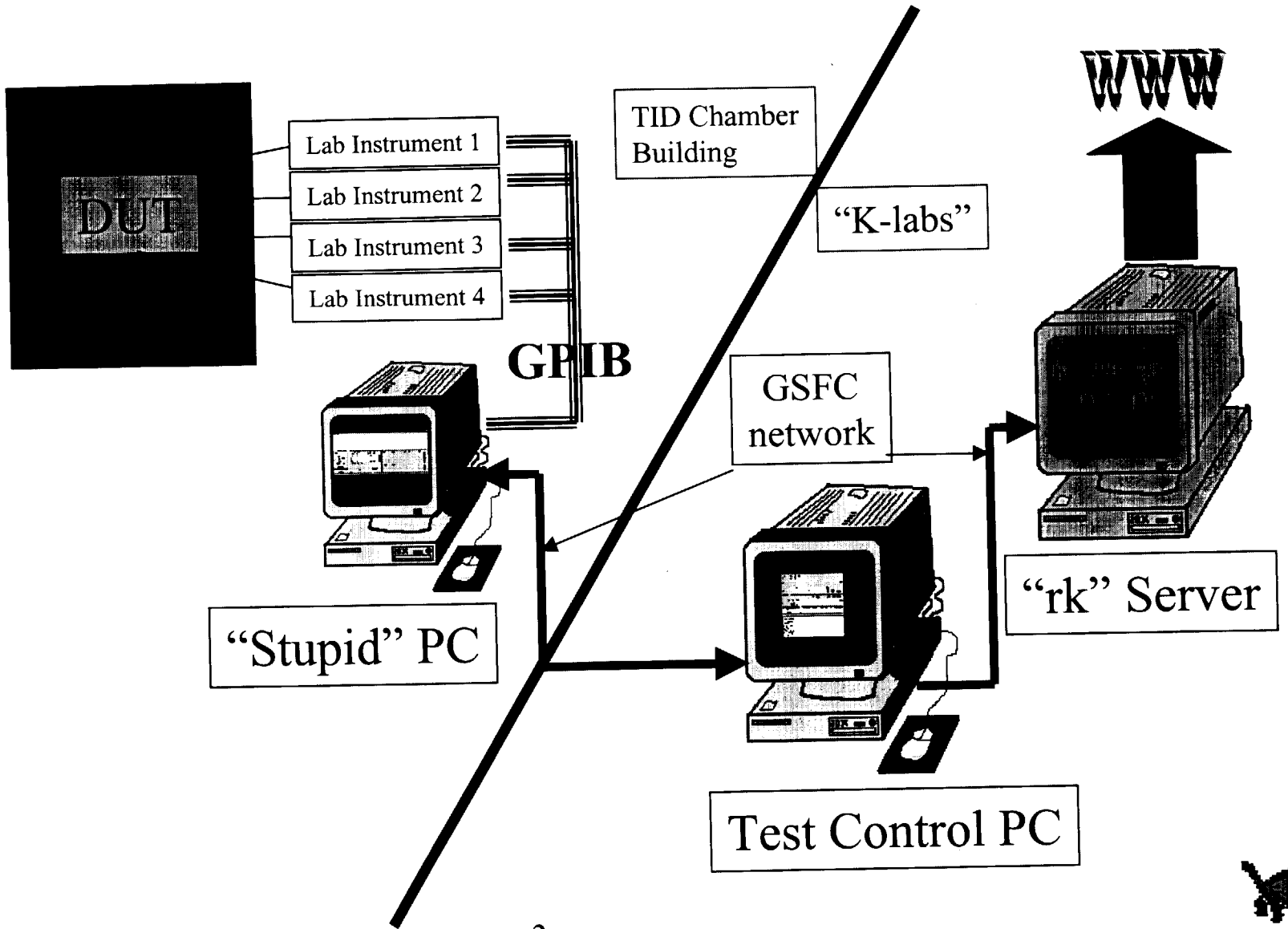
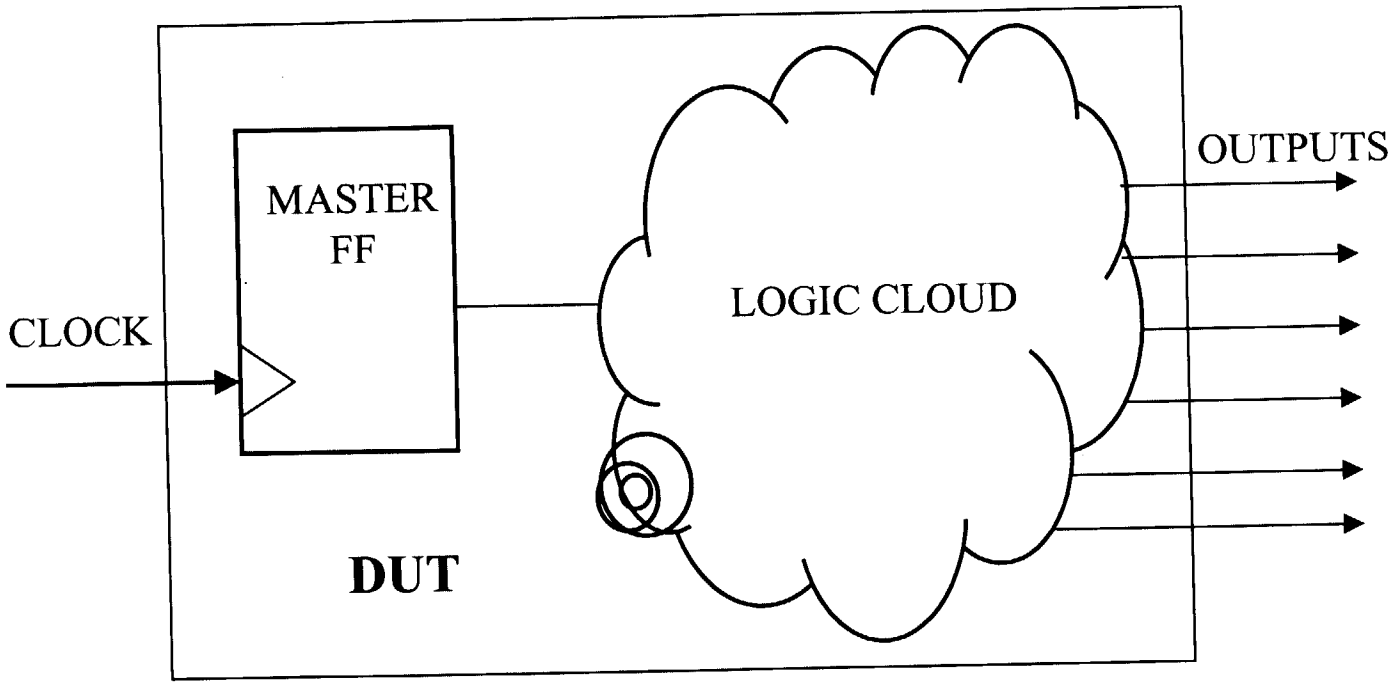
Overview

- Traditional TID effects testing of antifuse-based FPGA devices
- Modified test instrumentation and Device Under Test (DUT) programming patterns
- TID-induced damage in antifuse-based FPGA devices as a function of the state of bias of device's internal nodes
- Propagation delay TID-induced variations in antifuse-based FPGA devices
- Conclusions and lessons learned

GSFC Automated FPGA TID Test System



Traditional FPGA Pattern for TID Experiments at GSFC



Large (occupying most of the DUT) combinational circuit; controlled by the output of a single ("Master") Flip-Flop. Additional combinational and sequential logic not involved in *in situ* test is not shown

Previously Used FPGA TID Experiment Technique

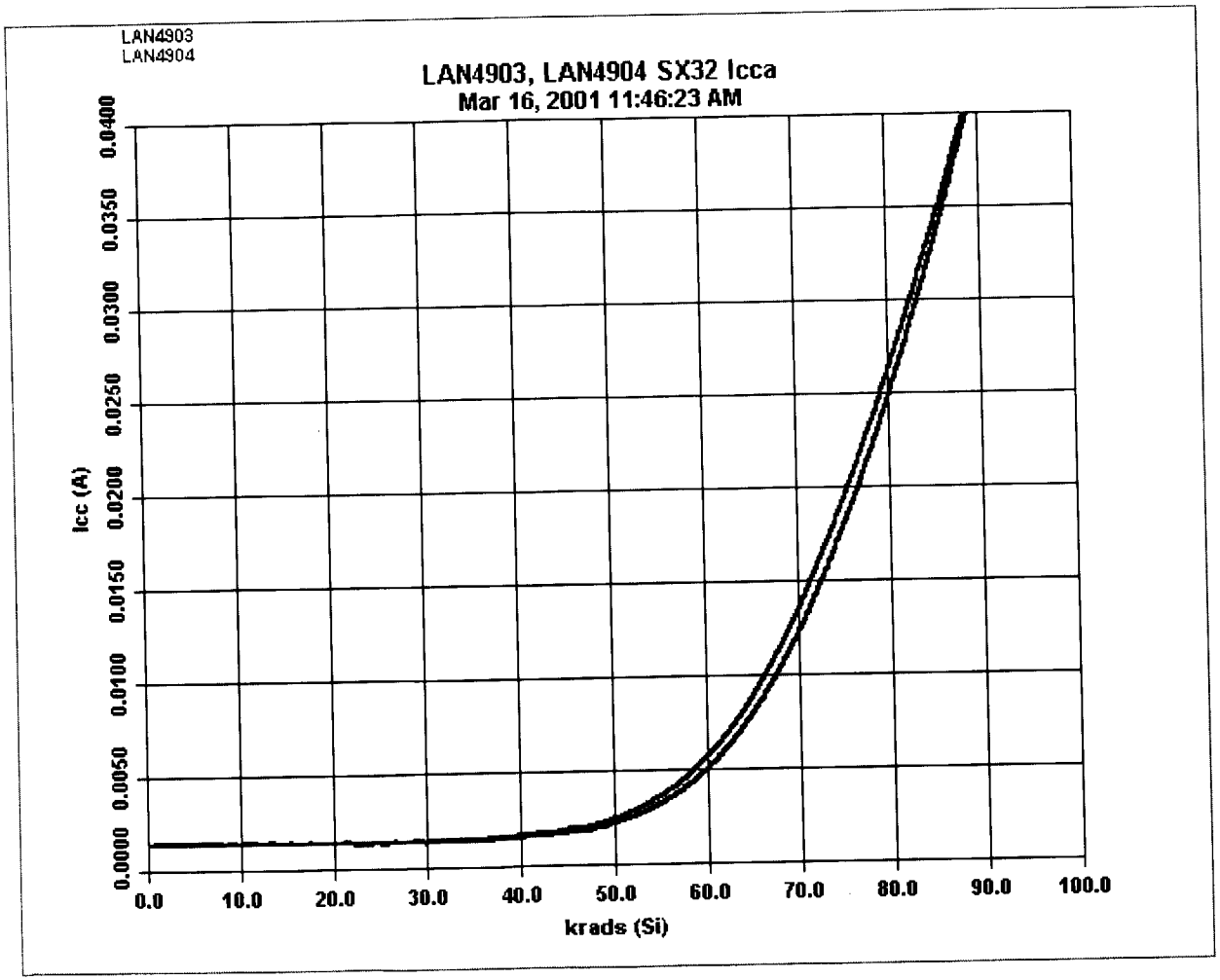
- DUT is irradiated in a certain "nominal" bias state for each of its internal nodes determined by the output of Master Flip-Flop
- Basic *in situ* functional test sequence is executed automatically every hour
  - Master flip-flop is toggled to invert the state of DUT's internal nodes and recording output voltages to verify inverted state
  - upon completion device is returned to its nominal state by clocking master flip-flop again
- Bias currents are monitored and recorded during irradiation process while device is in nominal state

Modification of FPGA TID Experiment Technique

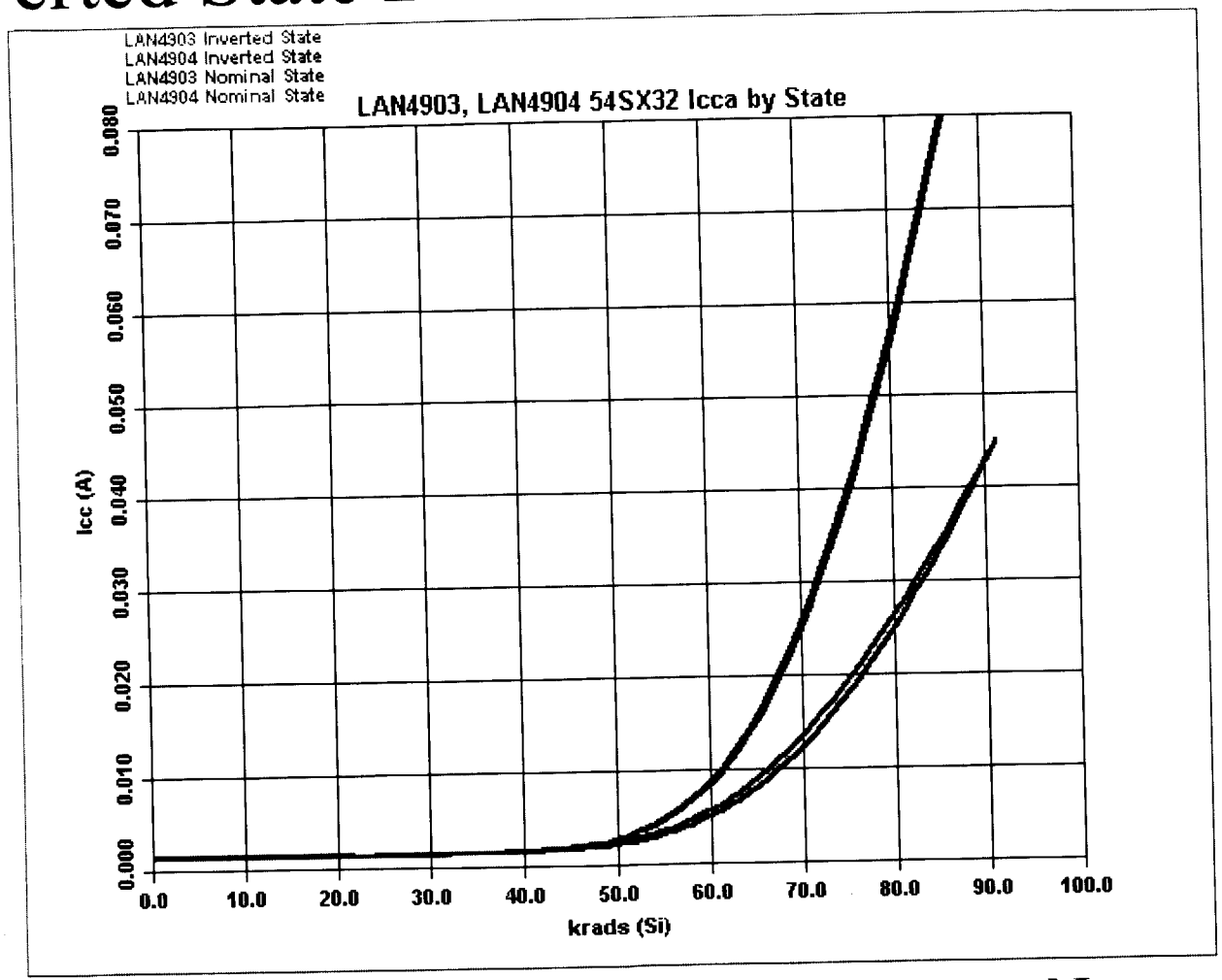
- Significant variation in leakage current as a function of logical state of the DUT's internal nodes observed for some devices of 54SX family during post-irradiation parametric testing

- *In situ* functional test expanded to include bias current recording for both nominal and inverted state for each execution of *in situ* functional test

Traditional I_{CC} TID chart - only nominal state measurements are recorded

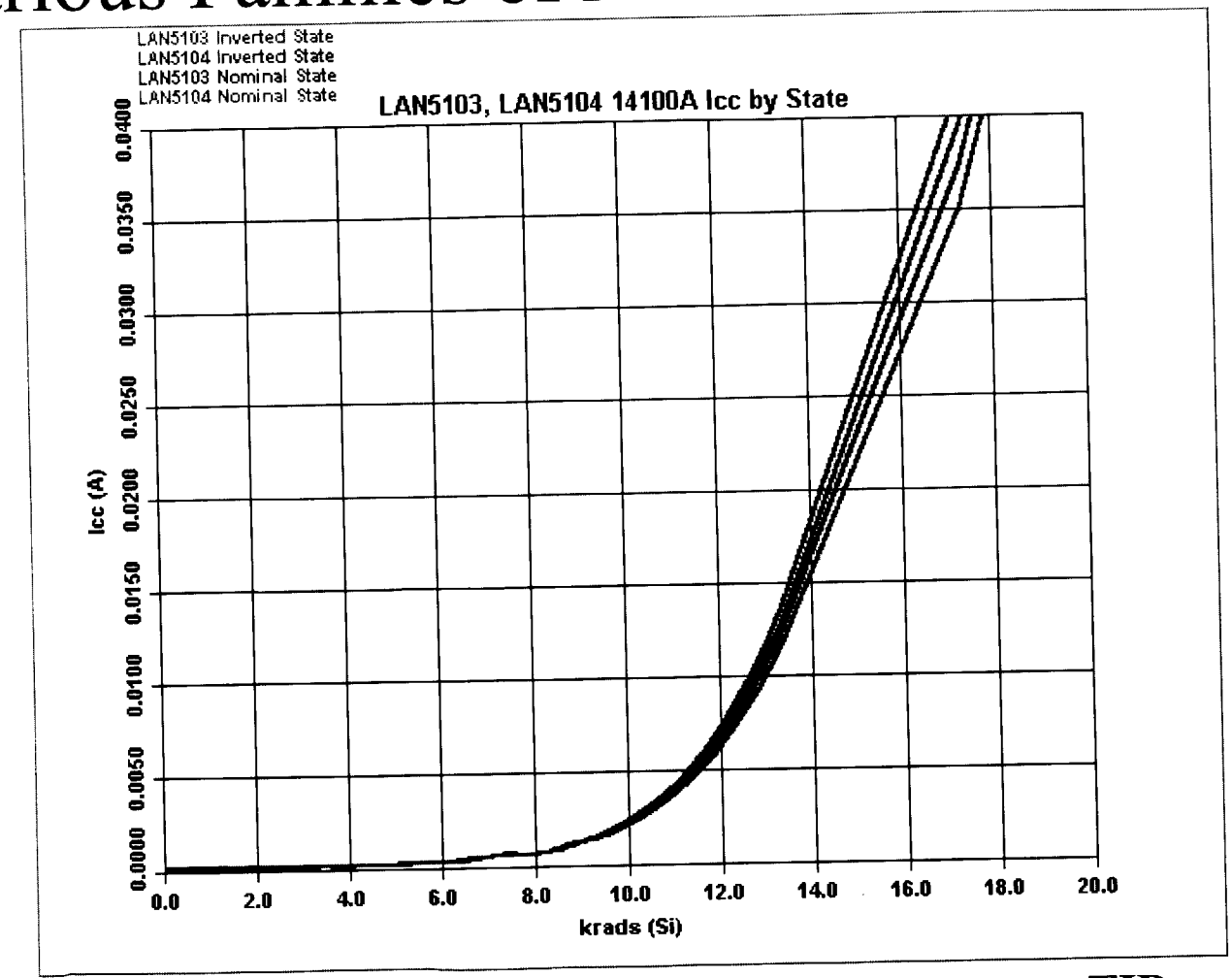


Modified Approach - both Nominal and Inverted State Bias Currents are Recorded



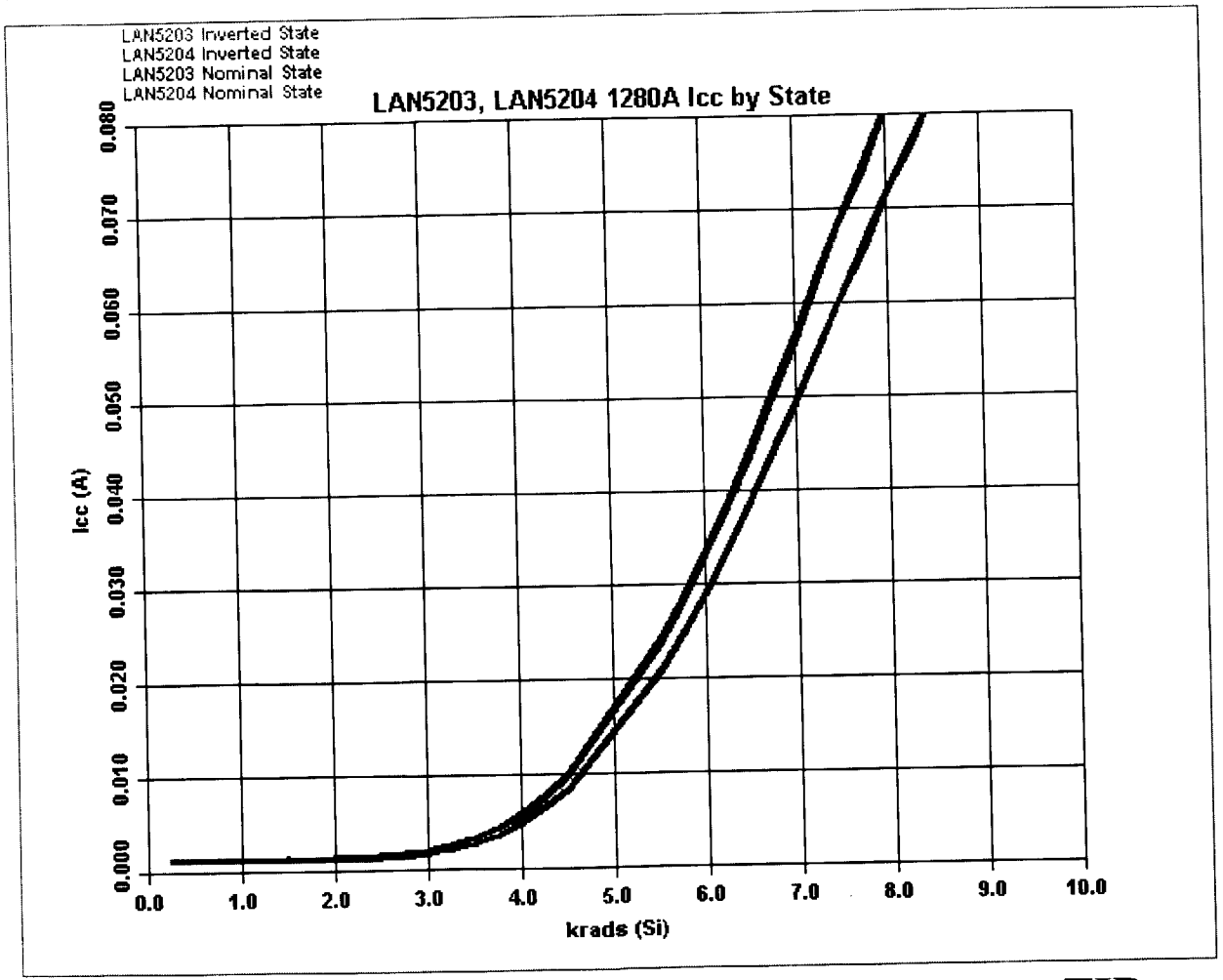
Significant (approximately twice) higher TID-induced I_{CC} leakage current for a device from 54SX32 family in inverted state as compared to nominal state of the device

Inverted and Nominal State Bias Currents for Various Families of Antifuse-based FPGAs



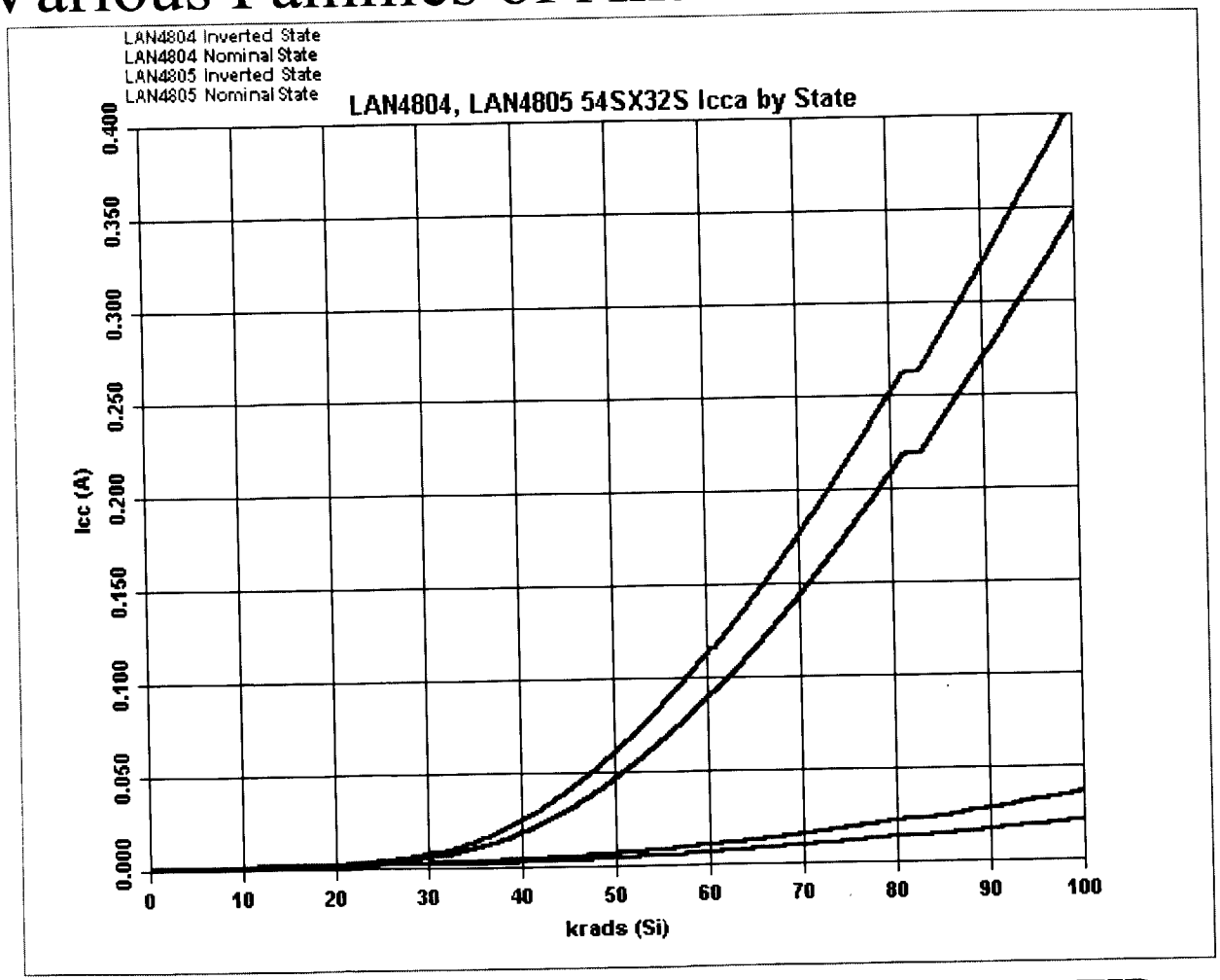
No significant variation in Inverted and Nominal state TID-induced ICC leakage for a device from A14100A family

Inverted and Nominal State Bias Currents for Various Families of Antifuse-based FPGAs



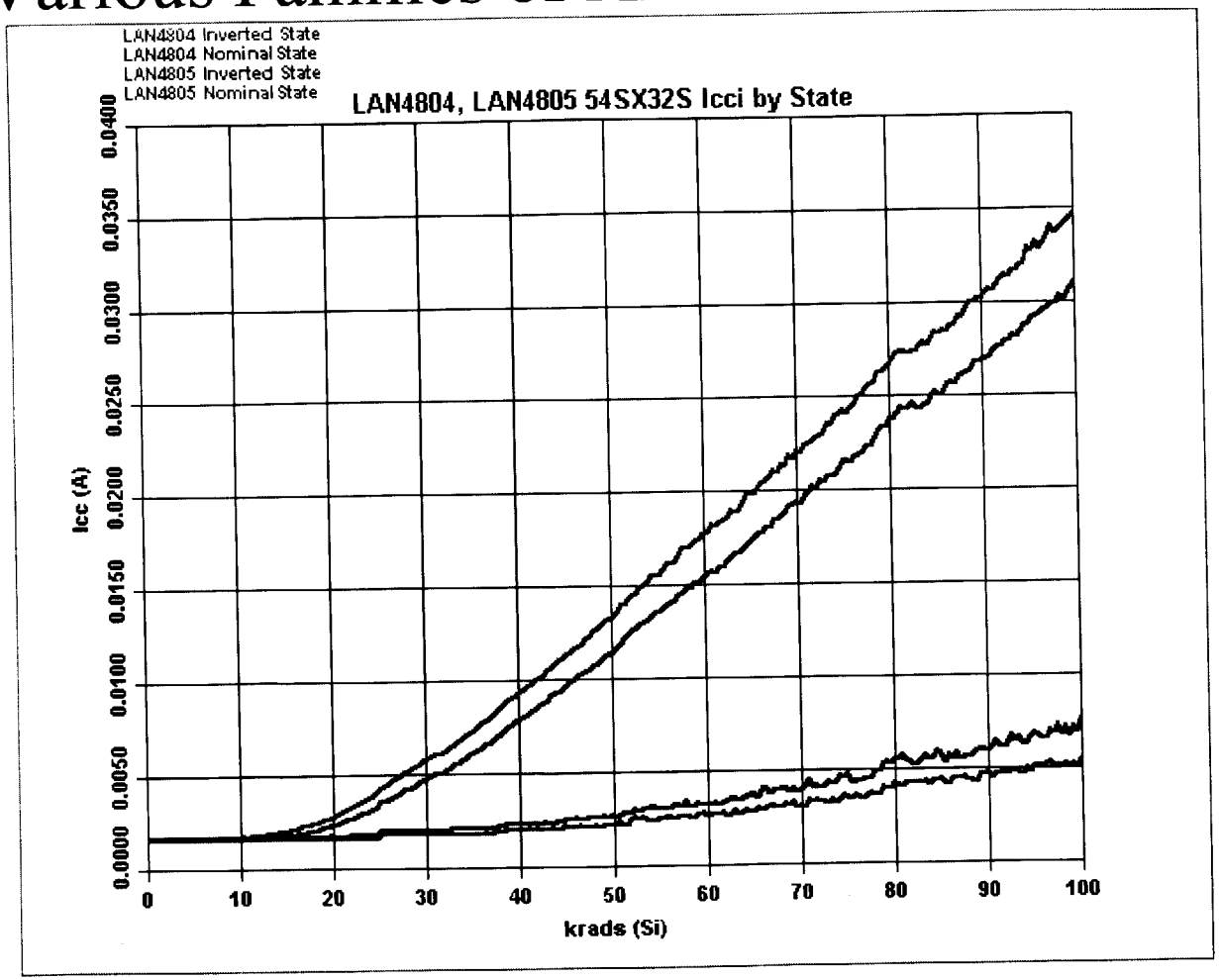
No significant variation in inverted and nominal state TID-induced I_{CC} leakage for a device from A1280A family

Inverted and Nominal State Bias Currents for Various Families of Antifuse-based FPGAs



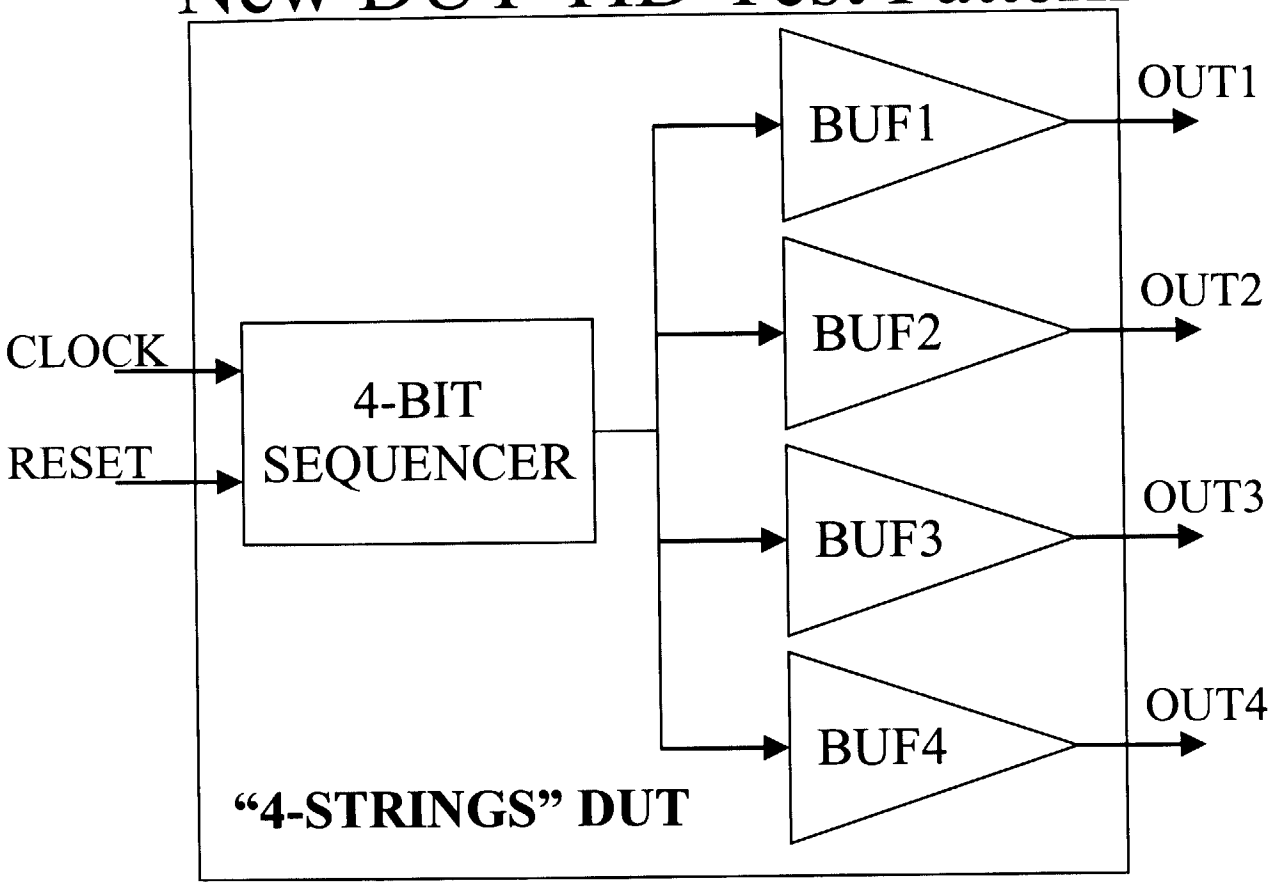
Significantly (approximately order of magnitude) higher TID-induced I_{CCA} leakage current for two devices from 54SX32S family in inverted state as compared to nominal state of a device

Inverted and Nominal State Bias Currents for Various Families of Antifuse-based FPGAs



Significantly (approximately order of magnitude) higher TID-induced I_{CCI} leakage current for two devices from 54SX32S family in Inverted state as compared to Nominal state of a device

New DUT TID Test Pattern

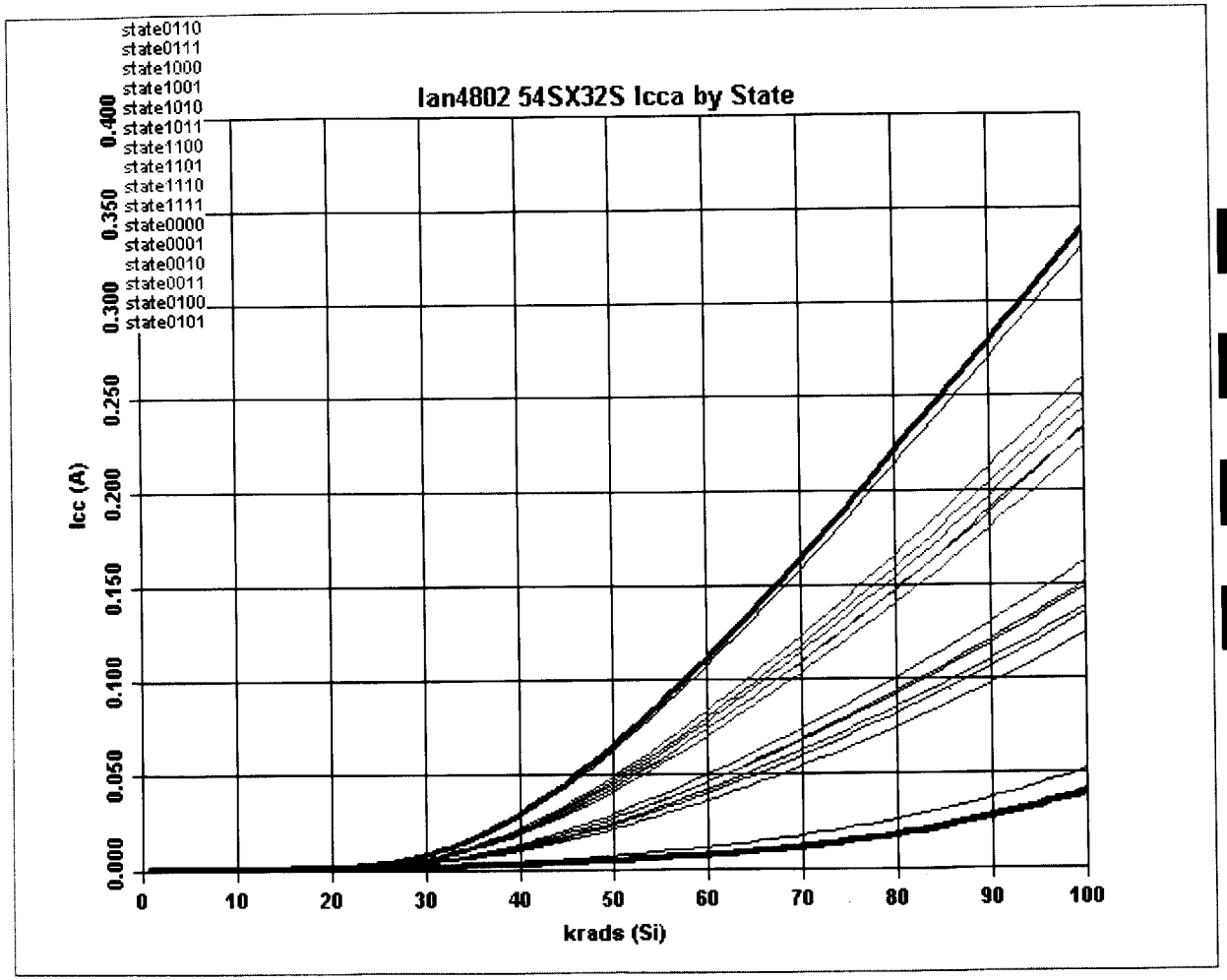


- BUF1 - string of 50 inverting buffers
- BUF2 - string of 500 inverting buffers
- BUF3 - string of 500 non-inverting buffers
- BUF4 - string of 500 non-inverting buffers

New TID *In Situ* Test Sequence

- During the irradiation the device is kept in a certain "nominal" state.
  - Typical Nominal State Configuration ("State 0101") :
    - Output 1 = High; Output 2 = Low; Output 3 = High; Output 4 = Low
- The controller is cycled through all sixteen states once each hour with the automated sequencing taking approximately 20 seconds
- The 4 strings of the DUT are put through through all possible combinations of biases.
- I_{CC} leakage is measured and recorded for all 16 combinations of biases

I_{CC} as a Function of TID and State of DUT for "4-Strings" Pattern



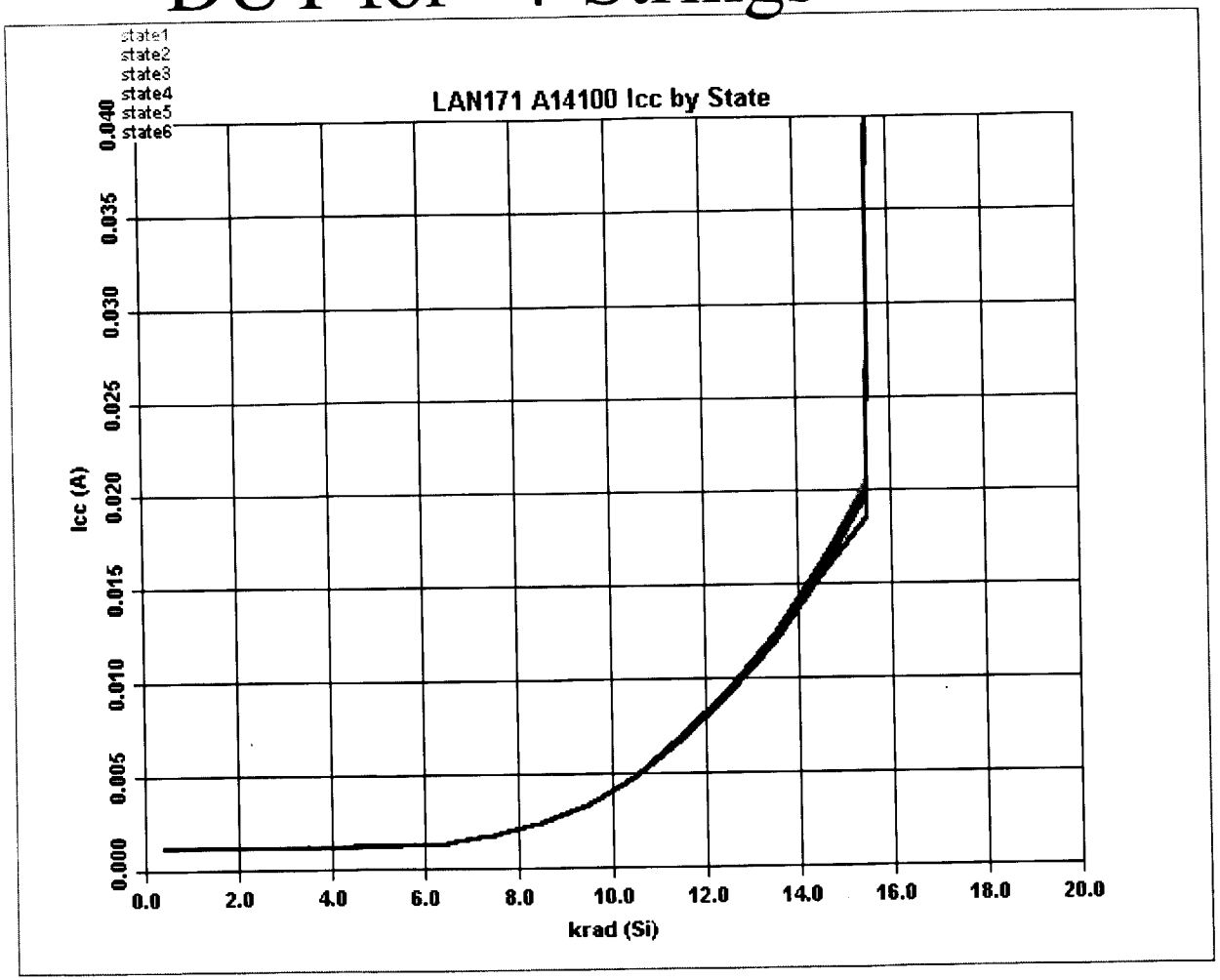
- All three "long" strings are in Nominal state
- One "long" string is in Inverted state
- Two "long" string are in Inverted state
- All three "long" string are in Inverted state

A "4-Strings" DUT from 54SX32S family: radiation-induced I_{CCA} leakage increases with the number of internal nodes placed in inverted state

I_{CC} of an Irradiated DUT as a Function of State of DUT for "4-Strings" Pattern

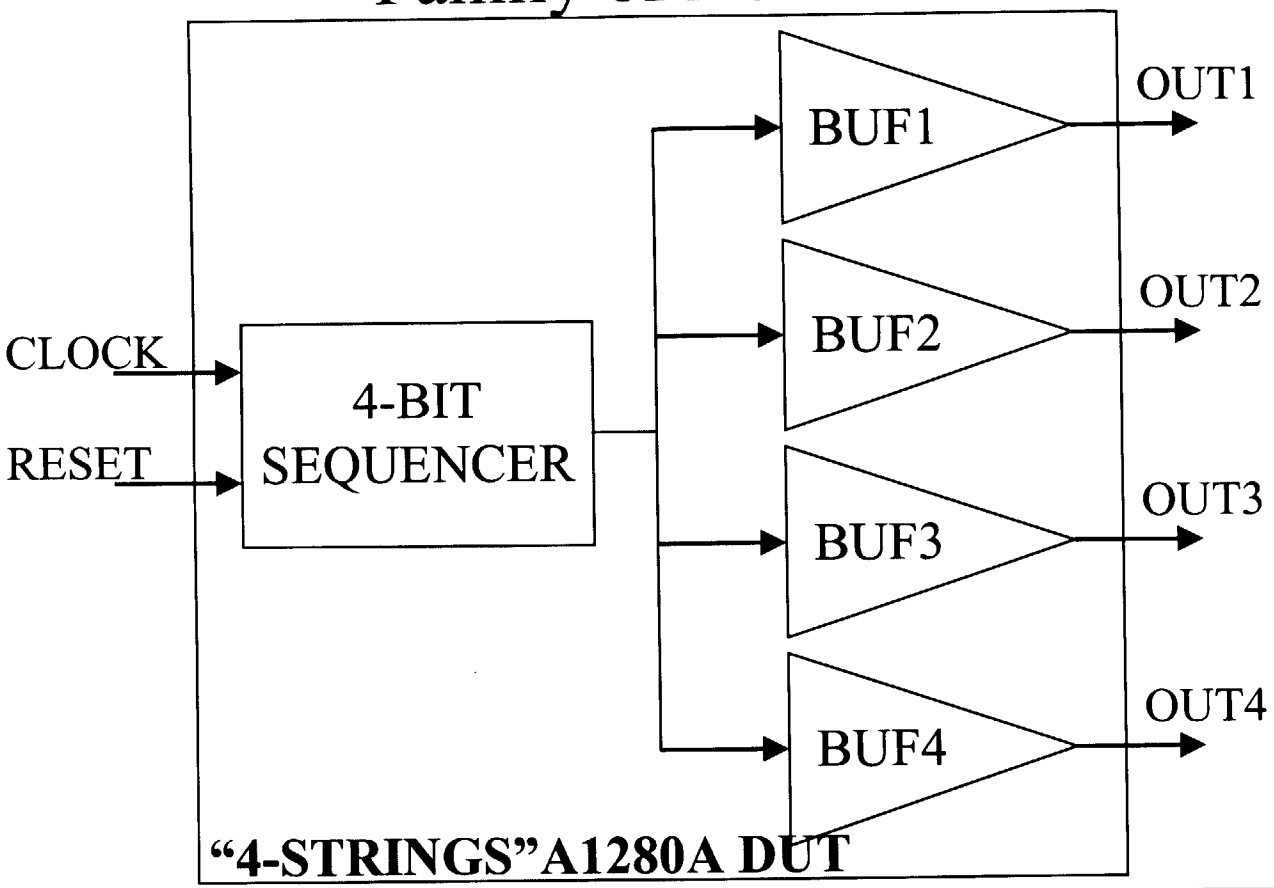
- The lowest I_{CC} leakage current for all tested devices of 54SX and 54SX-S families was consistently measured in the "nominal" state.
- Changing the bias of each string to the opposite of the nominal state caused an increase in the leakage current of the DUT in the amount proportionate to the number of nodes changing bias.
- Placing the device in the state with all strings biased inversely to their nominal states resulted in the additional leakage current approximately equal to the sum of current increases produced by individual string "flipping".
- The actual value of the "nominal" bias for the device nodes is not a significant factor affecting variations in bias current leakage; placing a node of a device in its inverted (whether logic high or low) state produces almost identical effect of leakage current increase

I_{CC} as a function of TID and State of DUT for "4-Strings" Pattern



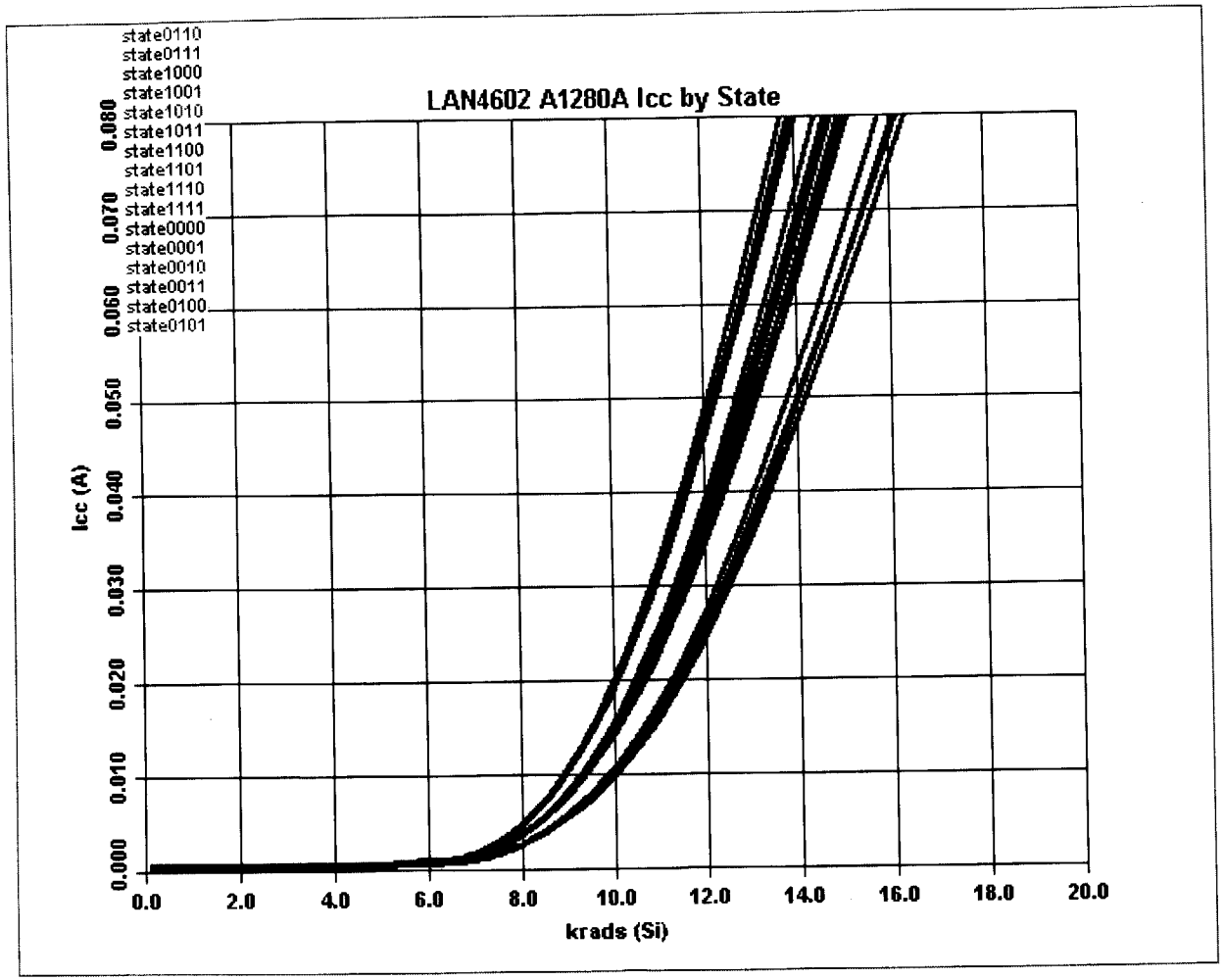
A "4-Strings" DUT from A14100A family: radiation-induced I_{CCA} leakage does not depend on the state of internal nodes of the DUT

Modification of 4-Strings Pattern for A1280A Family of Devices



- BUF1, BUF2, BUF3, BUF4 - strings of 400 non-inverting buffers
- BUF1 and BUF2- implemented by manually placing macros in C-modules
- BUF3 and BUF4 - utilize front-ends of S-modules with flip-flops bypassed

I_{CC} as a Function of TID and State of DUT for Modified "4-Strings" A1280A Pattern



Both S-module strings are in logic "low" state

One S-module string is in logic "high", another in logic "low" state

Both S-module strings are in logic"high" state

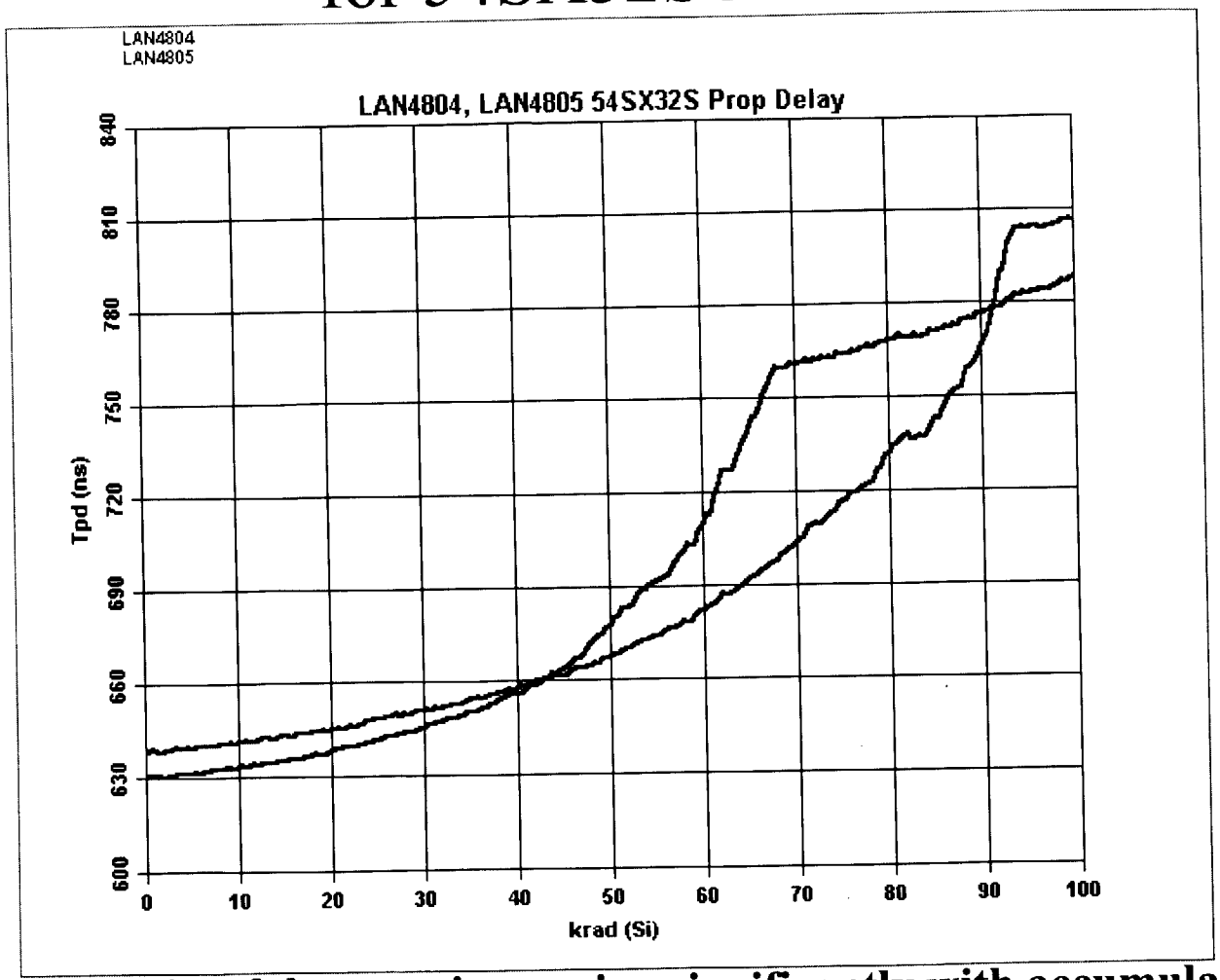
I_{CC} as a Function of TID and State of DUT for Modified "4-Strings" A1280A Pattern

- Changing the bias state for C-module-implemented strings did not produce any significant variations on the device's leakage current throughout the test.
- For the strings utilizing S-modules though, biasing a string to logic "high" level produced significant increase in leakage current in comparison with logic "low" bias of that string.
- Of the two strings using S-modules for logic implementation one was irradiated in nominal "low" bias state and the other one in nominal "high"; in both cases higher leakage currents were observed when strings were biased to logic "high" level.
- Placing both S-module strings in logic "high" state lead to the additional leakage current equal approximately the sum of the amounts produced by each string separately.

TID-induced Variations of Propagation Delay for 54SX32S Devices

- Propagation delay identified as a parameter potentially susceptible to TID-induced damage for devices of 54SX32S family
- *In situ* functional/parametric test sequence modified in order to study the effect
  - digitizing oscilloscope is is utilized to perform automated propagation delay measurement during each execution of *in situ* test
  - measurements recorded throughout the test along with regularly monitored parameters (e.g. bias currents, output voltages, etc)
- DUTs utilize traditional TID programming pattern

TID-induced Variations of Propagation Delay for 54SX32S Devices



Propagation delays are increasing significantly with accumulated TID, reaching 10% increase over original values in the 50 to 70 krad (Si) range for these two 54SX32S devices